IN THE CLAIMS:

Please **amend** claims 1, 2, 5 and 6 as follows:

1. (Amended) A semiconductor device with an MOS transistor, wherein a gate electrode of the MOS transistor is provided as a stacked structure comprising a silicon layer, a metal silicide layer, a reaction barrier layer and a metallic layer, formed in that order beginning with the silicon layer.

2. (Amended) A semiconductor device according to Claim 1, wherein the silicon layer is doped with an impurity of any desired conductivity type.

5. (Amended) A semiconductor device with an MOS transistor whose gate electrode is provided as a stacked structure comprising a silicon layer and a metallic layer as the uppermost layer thereof, wherein a metal silicide layer is provided on the silicon layer side and a reaction barrier layer is provided under the metallic layer side between the silicon layer and the metallic layer.

6. (Amended) A semiconductor device according to Claim 5, wherein the silicon layer is doped with an impurity of any desired conductivity type.

Please **cancel** non-elected claims 9-16 without prejudice or disclaimer but, however, applicants reserve the right to subsequently file a divisional application directed thereto.

Please **insert** new claims 17-32, as follows:

17. A semiconductor device according to claim 1, wherein the silicon layer is a polycrystalline silicon layer doped with an impurity of n-type or p-type conductivity.

18. A semiconductor device according to claim 4, wherein the silicon layer is a polycrystalline silicon layer doped with an impurity of n-type or p-type conductivity.

19. A semiconductor device according to claim 18, wherein the metal silicide layer has a thickness of 5-20 nm.

20. A semiconductor device according to claim 1, wherein the gate electrode is provided above a principal surface region of a semiconductor substrate, covering the spacing between a source region and drain region of the MOS transistor, the source and drain regions each having a first diffusion layer and a second diffusion layer, the second diffusion layer having a junction depth extended into the substrate deeper than that of the first layer.

21. A semiconductor device according to claim 20, wherein the silicon layer is a polycrystalline silicon layer doped with an impurity of n-type or p-type conductivity.

22. A semiconductor device according to claim 5, wherein the silicon layer is a polycrystalline silicon layer doped with an impurity of n-type or p-type conductivity.

23. A semiconductor device according to claim 8, wherein the silicon layer is a polycrystalline silicon layer doped with an impurity of n-type or p-type conductivity.

24. A semiconductor device according to claim 23, wherein the metal silicide layer has a thickness of 5-20 nm.

25. A semiconductor device with complementary MOS transistors, each MOS transistor having a gate electrode, a source region and a drain region, wherein the gate electrode is provided as a stacked structure comprising a silicon layer, a metal silicide layer, a reaction barrier layer and a metallic layer, formed in that order beginning with the silicon layer.

26. A semiconductor device according to claim 25, wherein the silicon layer of each MOS transistor gate electrode is a polycrystalline silicon layer doped with an impurity of one of an n-type and p-type conductivity for the gate electrode of a n-channel type MOS transistor and doped with an impurity of the other one of the n-type and p-type conductivity for the gate electrode of a p-channel type MOS transistor.

27. A semiconductor device according to claim 25, wherein the metal silicide layer has a thickness of 5-20 nm.

28. A semiconductor device according to claim 25, wherein the metal silicide layer is a tungsten silicide layer, the reaction barrier layer is a tungsten nitride layer, and the metallic layer is a tungsten layer.

29. A semiconductor device with complementary MOS transistors, each MOS transistor having a gate electrode, a source region and a drain region, wherein

the gate electrode is provided as a stacked structure comprising a silicon layer, an uppermost metallic layer, a metal silicide layer provided on the silicon layer side and a reaction barrier layer provided under the metallic layer side between the silicon layer and the metallic layer.

30. A semiconductor device according to claim 29, wherein the silicon layer of each MOS transistor gate electrode is a polycrystalline silicon layer doped with an impurity of one of an n-type and p-type conductivity for the gate electrode of a n-channel type MOS transistor and doped with an impurity of the other one of the n-type and p-type conductivity for the gate electrode of a p-channel type MOS transistor.

31. A semiconductor device according to claim 29, wherein the metal silicide layer is a tungsten silicide layer, the reaction barrier layer is a tungsten nitride layer, and the metallic layer is a tungsten layer.

32. A semiconductor device according to claim 29, wherein the metal silicide layer has a thickness of 5-20 nm.